## REMARKS

Applicants provide the present Amendment along with a Request for Continued Examination (RCE) to further clarify the recitations of the pending Claims in response to the Advisory Action of August 17, 2007 and the Final Office Action of May 30, 2007 (hereinafter, "Final Action"). No new matter has been added. Accordingly, Applicants respectfully request reconsideration of the pending claims for the reasons discussed below.

**The Section 112 Rejections**

Claims 1, 10, 11, and 21 stand rejected under 35 USC §112, first paragraph, as failing to comply with the enablement requirement. In particular, the Final Action asserts that the recitations of "comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step are not supported by the specification". Final Action, Page 2.

Applicants respectfully disagree. For example, as shown in Figures 3 and 4 of the present application, the nm memory cell arrays are designated by memory cell regions (1) to (8), the x-bit data is designated by each 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12, ODO13-16) output from each of the nm memory cell arrays (1) to (8), the nm-bit comparison result data is designated by MA1-8 generated by comparing each 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12, ODO13-16), the y-bit comparison result data is designated by ma1-ma4, and the y data I/O pads are designated by DQ1, DQ5, DQ9, and DQ13. *See*, for example, Specification, Figures 3 and 4.

Likewise, as shown in Figures 5 and 6 of the present application, the nm memory cell arrays are designated by memory cell regions (1) to (8), the x-bit data is designated by each 4-bit data (EDO1-4, EDO5-8, EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12, ODO13-16), output from each of the nm memory cell arrays (1) to (8), the nm-bit comparison result data is designated by MA1-8 generated by comparing each 4-bit data (EDO1-4, EDO5-8,

EDO9-12, EDO13-16, ODO1-4, ODO5-8, ODO9-12, ODO13-16), the y-bit comparison result data is designated by MAA1-MAA4, and the y data I/O pads are designated by DQ1, DQ5, DQ9, and DQ13. *See*, for example, Specification, Figures 5 and 6.

Accordingly, Applicants submit that the present specification as originally filed provides full support for the recitations of Claims 1, 10, 11, and 21. Thus, Applicants respectfully request withdrawal of the rejections of these claims and the claims dependent therefrom under 35 USC section 112, first paragraph.

In addition, Claims 1, 10, 11, and 21 stand rejected under 35 USC 112, second paragraph, as being indefinite. In particular, the Final Action asserts that it is "not clear what the (nmxx)-bit represents" and "whether the y-bit comparison result data is the y data I/O pads or not". Final Action, page 3.

In response, Applicants note that the "×" in the "(nm×x )-bit data" represents a multiplication sign. Also, as noted above, the "y-bit comparison result data" is designated by ma1-ma4 and/or MAA1-MAA4, and is thus different from the "y data I/O pads" designated by DQ1, DQ5, DQ9, and DQ13; however, the y-bit comparison result data is output through the y data I/O pads.

Accordingly, Applicants submit that the recitations of Claims 1, 10, 11, and 21 clearly point out and distinctly claim that which the applicant regards as the invention. As such, Applicants respectfully request withdrawal of the rejections of these claims and the claims dependent therefrom under 35 USC section 112, second paragraph.

**The Section 102 Rejections**

Claims 1-20 stand rejected under 35 USC §102(a) as being anticipated by Applicant Admitted Prior Art (U.S. Patent Application Publication No. 2004/0252549; hereinafter "AAPA"). Amended Claim 1, for example, recites:

> 1. A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:
>
> extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data

> write step; and
>
> comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. (*Emphasis added*).

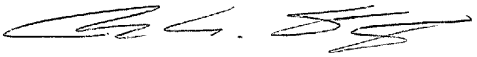
Applicants respectfully submit that the AAPA fails to disclose or suggest at least the test data read step of Claim 1, as highlighted above. For example, the AAPA discloses that the semiconductor memory device *simultaneously outputs* 8-bit comparison result data generated by comparing a total of 32-bit data of eight 4-bit data outputs from the nm memory cell arrays through 8 data I/O pads. *See* AAPA, Fig. 1. However, the present specification discloses that the semiconductor memory device generates 8-bit comparison result data generated by comparing a total of 32-bit data of eight 4-bit data output from the nm memory cell arrays and *sequentially outputs* 8-bit comparison result data by 4-bits in response to the control signal through 4 data I/O pads. *See* Specification, Fig. 3. Thus, the AAPA fails to disclose or suggest "comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and *sequentially* outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step", as recited in amended Claim 1.

Accordingly, Applicants respectfully submit that the AAPA fails to disclose or suggest at least the recitations of Claim 1 highlighted above. Thus, Applicants submit that Claim 1 is patentable for at least the above reasons. Claims 10, 11, and 21 include similar method and device recitations, and as such, are patentable for at least similar reasons. Also, dependent Claims 2-3 and 12-13, and 36-41 are patentable at least per the patentability of Claims 1, 10, 11, and 21 from which they depend.

**Conclusion**

Accordingly, based on the remarks provided above, Applicants respectfully submit that all of the pending claims are now in condition for allowance. Thus, Applicants respectfully request withdrawal of the outstanding rejections, allowance of the pending claims, and passing the application to issue. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,



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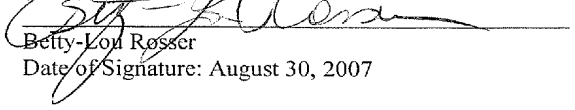

Betty-Lou Rosser
Date of Signature: August 30, 2007